HIGH-SPEED LOW-COST DIRECT CONVERSION DIGITAL RECEIVER

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***Abstract* — In this paper, an analog carrier recovery loop is proposed and developed to provide a complete direct conversion digital six-port receiver operating at microwave ISM frequency of 2.45 GHz. Results on data rate limitation are shown for QPSK signals up to data rates of 52 Mb/s. Parametric measurements in connection with CW, adjacent channel and co-channel interferences are presented for a data rate of 40Mb/s. Finally, phase offset between the carrier and the reference signal, along with carrier frequency deviation performance are also presented for a rate of 40Mb/s.**

I. INTRODUCTION

Robust and low cost digital receivers with low power consumption are required for expanding wireless mass-market communications. Such receivers, with several megabits per second data transmission capacity, will be needed for the new generation of cellular Internet multi-media services. A six-port direct conversion digital receiver operating at millimeter wave frequencies was first proposed a number of years ago [1]. More recently, microwave direct conversion six-port software receivers operated with DSPs have been investigated to satisfy the requirements of the next generation 3G cellular communications system [2,3]. In addition, a six-port direct conversion hardware receiver architecture was recently proposed as means to avoid more costly software receivers using DSPs [4]. However, no solution was then offered for a carrier recovery circuit. In this paper, an analog carrier recovery loop is proposed to provide a complete hardware direct conversion digital six-port receiver that operates at microwave ISM frequency of 2.45 GHz.

Results on the data rate limitation, interferences signals suppression, phase offset between the carrier and the reference signal are given with the analog carrier recovery module in operation. Standard QPSK modulation format is used with data rates up to of 52 Mb/s. Two independent pseudo-random NRZ pulse trains of equal rate are used to generate the QPSK signal and pulse shaping filters were not used prior to modulation with a vector signal generator.

II. PROTOTYPE RECEIVER

To start with, Fig. 1 presents a block diagram of the proposed receiver's architecture, including a carrier recovery module under study. The RF filters and the variable gain LNA were not implemented in this investigation.

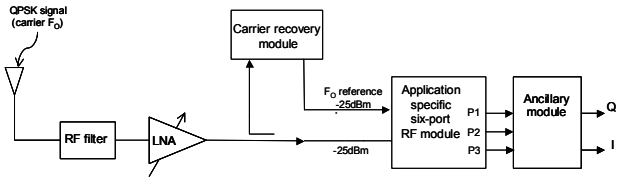

Figure 1: Direct conversion six-port type high-speed digital receiver architecture.

Fig. 2 shows our six-port circuit with the input signal, input reference signal (LO) and three RF ports feeding Schottky diode matching circuits that provide the base band signals, denoted as P_1, P_2 and P_3.

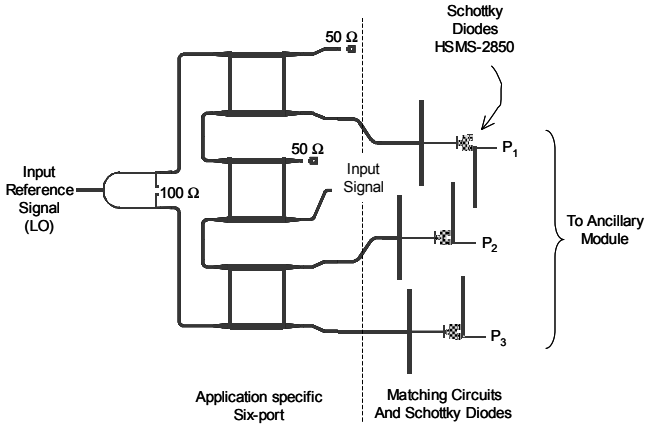

Figure 2: Layout of application specific six-port RF module.

Fig. 3 depicts our wideband (30MHz) ancillary module circuit with operational amplifiers and a QPSK decoder using two high-speed comparators fed directly from the output of video amplifiers.

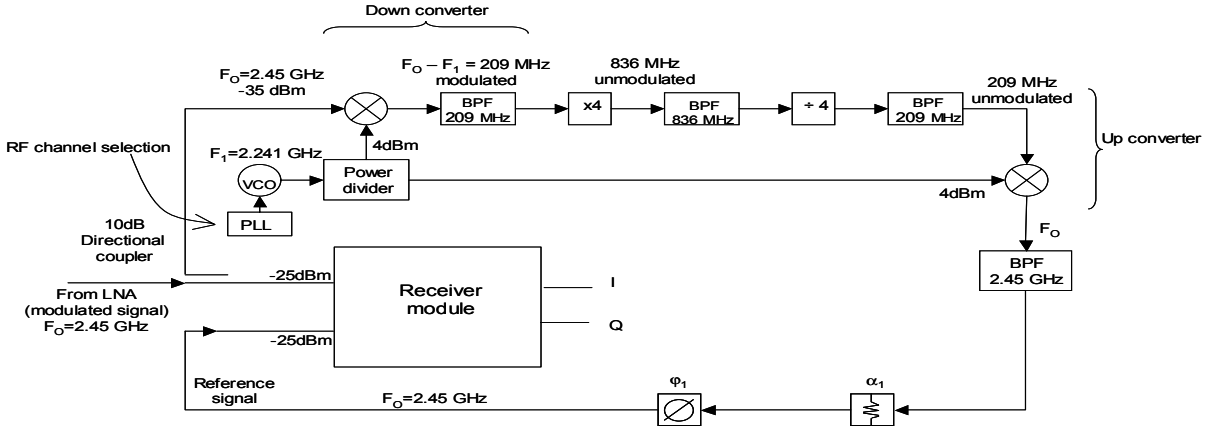

Figure 4: Complete description of the carrier recovery module.

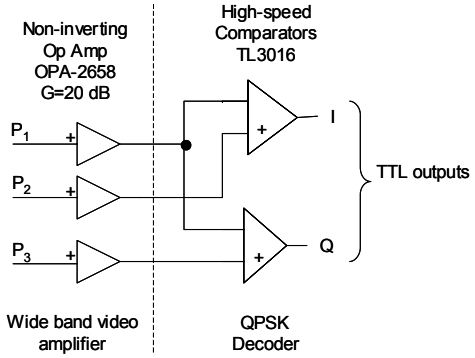

Figure 3: Ancillary circuit module.

The carrier recovery module circuit, as described in Fig. 4, is designed to recuperate the carrier frequency F_o and provides the required reference signal for the six-port. A 10dB coupler samples the input signal with the carrier at F_o=2.45GHz, providing a modulated signal to the RF input of the down converter at a power level of -35dBm. A CW signal (4dBm) is fed into the down converter LO input from a channel select oscillator operating at frequency F_1=2.241GHz. The modulated down converted signal (F_o - F_1) is filtered, frequency multiplied (x4) and frequency divided (÷4) such as to provide an unmodulated signal at (F_o - F_1) = 209MHz. This CW signal is upconverted by mixing with F_1=2.241GHz CW signal to exactly recover the carrier frequency (F_o). The resulting F_o=2.45GHz CW signal is then fed to the reference input of six-port at a power level of -25dBm using appropriate attenuation (α_1) and phase shift (φ_1).

The times-four frequency multiplier is realized with a single BJT transistor and provides 10dB of conversion loss. The divide-by-four circuit is a commercial prescaler chip with a fixed division ratio and a sensitivity of -20dBm.

III. Test Results

Fig. 5 shows results of BER measurements versus data rate with the carrier recovery circuit in operation compared to results obtained for the same measurements with the reference signal locked to the carrier signal (both from the same generator).

It is seen that the carrier recovery circuit degrades the maximum data transmission rate from 66Mb/s, when both the carrier and reference signals are synchronous, to a lower transmission rate of 46Mb/s when the carrier recovery loop is used. Since the carrier recovery module is limiting the data rate, the following measurements have been done at a rate of 40Mb/s.

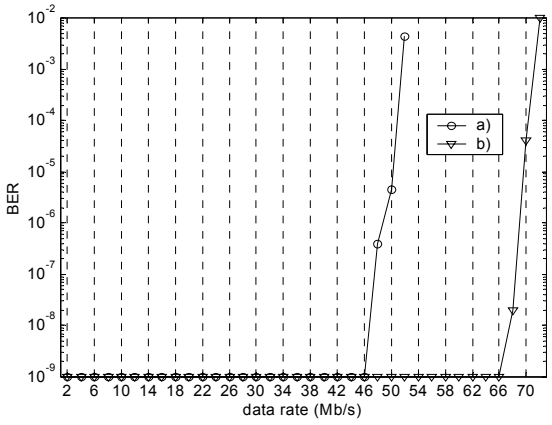

Figure 5: Measured results of BER vs. data rate: a) with carrier recovery circuit; and b) without carrier recovery circuit (both signals from same generator are synchronous).

Measurements results of BER versus power of CW interference (P_{Int}) normalized to the power level of carrier ($P_{carrier}$) for various frequency offsets between the carrier

and the interference tone are presented in Fig. 6. It is seen that for a frequency offset of 100MHz, the resulting second order mixing product at base band is well above the cut-off frequency of ancillary module (30MHz), therefore the power of interference tone can be at least 12dB higher than for a frequency offset of 20MHz and 30MHz (within or near the band edge of ancillary module).

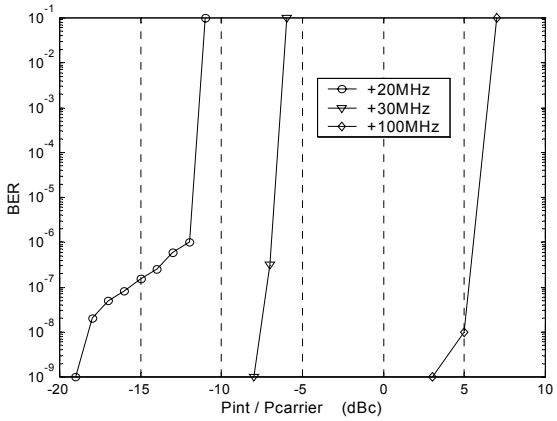

Figure 6: Robustness of carrier recovery loop to interference tone offset from carrier frequency.

BER measurements in the presence of an adjacent channel are given in Fig. 7. The adjacent channel carrier frequency is set 44MHz above the main channel. This leaves 4MHz between the edges of modulated channels. Both channels are QPSK modulated with a data rate of 40Mb/s and uncorrelated. It is noted that no RF filtering is used prior to feeding both signals to the input of six-port circuit.

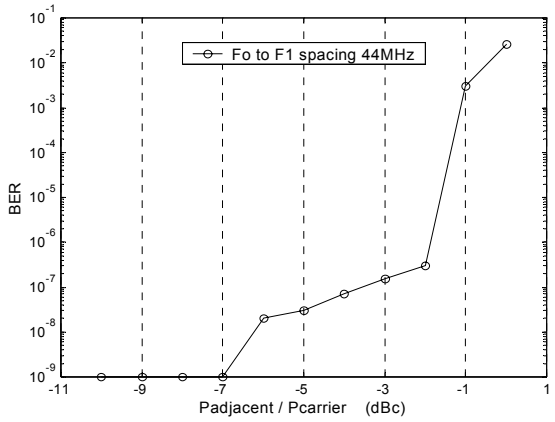

Figure 7: BER in the presence of an adjacent channel.

Fig. 8 shows BER measurements this time with a co-channel interference. The interference signal is again QPSK modulated with a data rate of 40Mb/s and not correlated to the main signal. These results indicate a rapid decay of transmission quality between $P_{co\text{-}channel}/P_{carrier}$ = -20dBc and -19.5dBc.

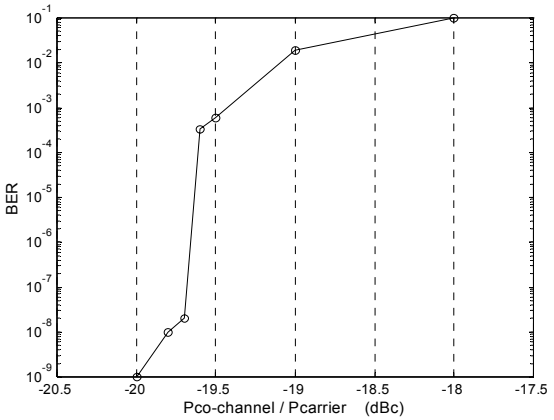

Figure 8: Measured BER with a co-channel interferer.

Fig. 9 presents results of BER versus phase difference between carrier and reference signal (LO) with the carrier recovery circuit and with the carrier frequency locked to the reference signal (both signals derived from the same source are synchronous). It is observed that the carrier recovery loop is not affected by phase differences between the carrier and the reference signal.

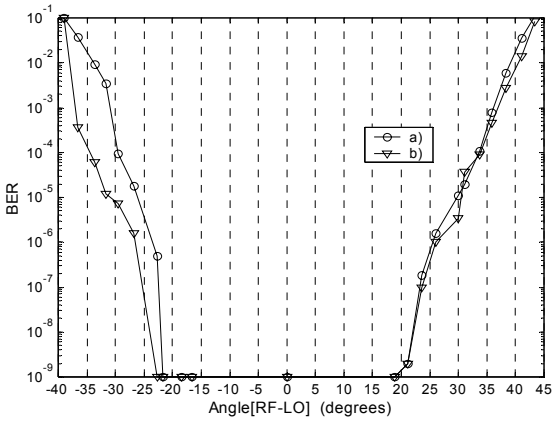

Figure 9: BER vs phase difference between reference and carrier signal for data rate of 40Mb/s: a) with carrier recovery; and b) without carrier recovery (both signals from same generator).

In a separate test, it was found that the recovery loop is operational with 40Mb/s data rate on a frequency modulated carrier using Marconi 2031 generator. Fig. 10 demonstrates signal generation block diagram for this test.

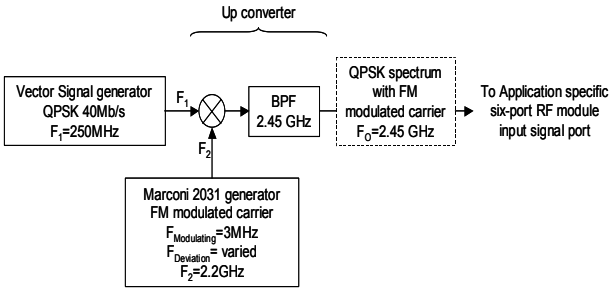

Figure 10: RF signal generation with additionnal FM modulation applied to carrier.

Measurements results of BER against increasing frequency deviation for a fixed modulating rate of 3MHz are shown in Fig. 11. These results indicate that the architecture is tolerant to rapid carrier frequency shifts as may be encountered in various communication systems [5]. A BER of 10^{-6} is attained at a frequency deviation of 8000 KHz for a 3 MHz modulating rate.

These last measurements are an indirect evaluation of locking time and suggest applicability of this architecture to applications requiring fast carrier synchronization like frequency hopping and burst communication systems.

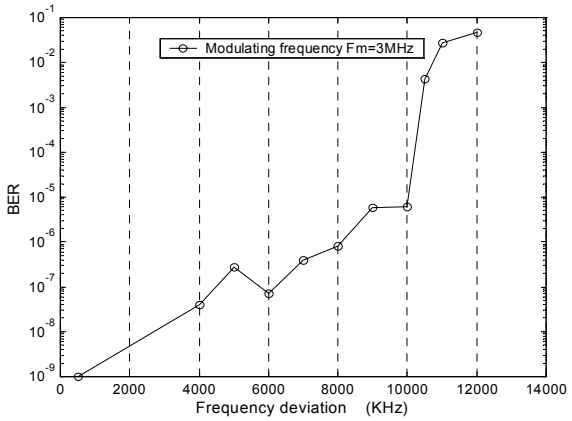

Figure 11: Measured BER vs carrier frequency deviation.

IV. Conclusion

An application specific six-port architecture has been proposed and tested with a carrier frequency of 2.45GHz and a QPSK modulation format.

Measured results indicate a possibility of developing a highly integrated, totally analog, high-speed receiver that consists of an RF module and a base-band module including the carrier recovery circuit.

Acknowledgement

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References

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